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EXAMINER

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/518,779	Applicant(s) GOPALAKRISHNAN ET AL.	
	Examiner SARAH K. SALERNO	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 May 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-39 and 43-45 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-39 and 43-45 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Applicant's amendment/arguments filed on 5/24/2010 as being acknowledged and entered. By this amendment claims 40-42 are canceled, no claims have been added claims 1-39 and 43-45 are pending and no claims are withdrawn.

The Non-Final rejection of claims 1-39 and 43-45 in the Non-Final office action dated 02/22/2010 are withdrawn based on applicants arguments.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-7, 9-17, 18-20, 30-37, 39 and 43-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto (US PGPub 2002/0117689 of record) in view of Baba et al. (US Patent 5,686,739) and Yee et al. (US Patent 5,736,890).

Claim 1: Akimoto teaches a semiconductor device, comprising: a multi-region body including a first region (22) dominated by charge carriers of a first polarity that extends to a first junction, a second region (23) dominated by charge carriers of a second polarity, opposite the first polarity, that extends to a second junction, and an intermediate region (24) having an effective length extending from the first junction to the second junction; and a gate (20) located over one of the junctions and laterally

offset from the other junction, capacitively-coupled to the body FIG. 1A-1B; [0071-0072]).

Akimoto does not teach a control circuit configured to apply a control signal, when the body is reversed biased, to modulate the effective length of the intermediate region to a nonzero value by changing a concentration of carriers in a portion of the intermediate region extending from the second junction and offset from the first junction. Baba teaches applying a control signal when the body is reversed biased, to modulate the effective length of the intermediate region to a nonzero value by changing a concentration of carriers in a portion of the intermediate region extending from the second junction and offset from the first junction (Col. 2 lines 1-35) creating a channel in the device when the voltage is applied. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied a control signal to the device of Akimoto when the body is reversed biased, to modulate the effective length of the intermediate region to a nonzero value by changing a concentration of carriers in a portion of the intermediate region extending from the second junction and offset from the first junction, creating a channel in the device as taught by Baba (Col. 2 lines 1-35).

Akimoto and Baba do not teach a control circuit configured to apply a control signal. Yee teaches a control circuit configured to apply a control signal to the control/gate electrode to operate the transistor (Col. 2 lines 55-67 and Clm 1). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Akimoto and Baba to have a

control circuit to apply the control signal to the gate so that the transistor can operate as taught by Yee (Col. 2 lines 55-67 and Clm 1).

Claim 2: Akimoto, Baba and Yee teach the control circuit is further configured to apply the control signal to cause the device to transition between a current-conducting state in which the device is in an avalanche breakdown condition and a current-blocking state (Col. 2 lines 55-67 and Clm. 1).

Claim 3: Akimoto (FIG. 1A-1B; [0071-0072]), Baba, and Yee (Col. 2 lines 55-67 and Clm. 1) teach the gate and control circuit are configured to modulate an electric field within the body to cause the device to transition between a current- conducting state in which the device is in avalanche breakdown condition and a current-blocking.

Claim 4: Akimoto, Baba and Yee teaches the control circuit is configured to apply a relatively high bias voltage at the gate to maintain the device in a current-conducting state in which the device is in an avalanche breakdown condition, and apply a relatively low bias voltage at the gate to maintain the device in a current-blocking state (Col. 2 lines 55-67 and Clm 1).

Claim 5: Akimoto, Baba and Yee teach the control circuit is configured to apply the relatively high bias voltage to shorten the effective length of the intermediate region (Col. 2 lines 55-67 and Clm 1).

Claim 6: Akimoto, Baba and Yee teach the control circuit is configured to apply a relatively low bias voltage at the gate to maintain the device in a current-conducting state in which the device is in an avalanche breakdown condition, and a relatively-high

bias voltage at the gate to maintain the device in a current-blocking state region (Col. 2 lines 55-67 and Clm 1).

Claim 7: Akimoto, Baba and Yee teach the control circuit is configured to apply the relatively low bias voltage to shorten the effective length of the intermediate region (Col. 2 lines 55-67 and Clm 1).

Claim 9: Akimoto teaches the gate is located at least predominantly over the intermediate region (FIG. 1A-1B; [0071-0072]).

Claim 10: Akimoto teaches the gate is located to provide a surface channel nearer the second junction than the first junction (FIG. 1A-1B; [0071-0072]).

Claim 11: Akimoto, Baba and Yee teaches wherein when the body is reversed-biased, the control circuit is configured to apply the control signal to maintain the first region at a relatively lower voltage level than the second region, the difference in potential of the first and second regions being sufficient to cause a breakdown condition in the intermediate region in response to the control signal modulating the length of the intermediate region and thereby reducing the distance across the intermediate region over which the potential drops (Col. 2 lines 55-67 and Clm 1).

Claim 12: Akimoto teaches the intermediate region has a polarity that is neutral relative to the polarity of the first and second regions (FIG. 1A-1B; [0071-0072]).

Claim 13: Akimoto teaches the intermediate region is lightly doped to achieve the polarization of one of the first and second regions, the intermediate region having a substantially lower dopant concentration level, relative to said one of the first and second regions (FIG. 13).

Claim 14: Akimoto teaches the intermediate region is substantially intrinsic (FIG. 1A-1B; [0071-0072]).

Claim 15: Akimoto (FIG. 1A-1B; [0071-0072]), Baba, and Yee (Col. 2 lines 55-67 and Clm. 1) Akimoto, Baba and Yee teach the control circuit and gate are further adapted to cause the device to transition between a current-conducting state in which the device is in an avalanche breakdown condition and a current-blocking state in which substantially no leakage current passes between the first and second regions drops.

Claim 16: Akimoto (FIG. 1A-1B; [0071-0072]), Baba and Yee (Col. 2 lines 55-67 and Clm 1) teach the control circuit is configured for applying the control signal to change the concentration of carriers in the intermediate region.

Claim 17: Akimoto (FIG. 1A-1B; [0071-0072]) and Yee (Col. 2 lines 55-67 and Clm 1) teach the control circuit and gate are further adapted to increase an electric field in the intermediate region and for causing an avalanche breakdown condition drops (FIG. 1A-1B; [0071-0072]).

Claim 18: Akimoto teaches a semiconductor device comprising:
a multi-region body including a P-type region (23), an N-type region (22) and an intermediate region (20) having a first junction with the P-type region and a second junction with the N-type region, the body adapted to be reverse biased across the P-type and N- type regions; a gate (20) coupled via an intervening gate dielectric material to the intermediate region, located over one of the junctions and laterally offset from the other junction to present an electric field substantially at only one of the two junctions(FIG. 1A-1B; [0071-0072]).

Akimoto does not teach a control circuit configured to apply a voltage-bias control signal to the gate to control the gate, the P-type region and the N-type region to switch the device between at least two stable conductance states. Baba teaches applying a voltage-bias control signal when the body is reversed biased, to modulate the effective length of the intermediate region to a nonzero value by changing a concentration of carriers in a portion of the intermediate region extending from the second junction and offset from the first junction (Col. 2 lines 1-35) creating a channel in the device when the voltage is applied. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied a voltage-bias control signal to the device of Akimoto when the body is reversed biased, to modulate the effective length of the intermediate region to a nonzero value by changing a concentration of carriers in a portion of the intermediate region extending from the second junction and offset from the first junction, creating a channel in the device as taught by Baba (Col. 2 lines 1-35).

Akimoto and Baba do not teach a control circuit configured to apply a control signal. Yee teaches a control circuit configured to apply a voltage-bias control signal to the control/gate electrode to operate the transistor (Col. 2 lines 55-67 and Clm 1). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Akimoto and Baba to have a control circuit to apply the control signal to the gate so that the transistor can operate as taught by Yee (Col. 2 lines 55-67 and Clm 1).

Claim 19: Akimoto, Baba and Yee teach the control circuit applies the voltage-bias control signal to the gate to switch the device between a high-resistance conductance state and a low-resistance conductance state by causing an avalanche breakdown condition at a field-induced junction in the intermediate region (Col. 2 lines 55-67 and Clm 1).

Claim 20: Akimoto teaches the intermediate region has a length that separates the first and second junctions sufficiently to permit the avalanche breakdown condition before another breakdown condition when the body is reverse biased (FIG. 1A-1B; [0071-0072]).

Claim 30: Akimoto teaches a memory circuit comprising: a data storage node; first and second multi-region bodies, each body including a first region dominated by charge carriers of a first polarity that extends to a first junction, a second region dominated by charge carriers of a second polarity opposite the first polarity that extends to a second junction, and an intermediate region having an effective length extending from the first junction to the second junction; a first gate coupled to the first multi-region body via an intervening dielectric material and offset for using a control signal, when the first body is reversed biased, to present an electric field substantially at only one of the first and second junctions of the first body, a second gate coupled to the data storage node and to the second body via an intervening dielectric material and adapted for using a charge at the data storage node, when the second body is reversed biased, to modulate an electric field in the intermediate region of the second body, the second body responding to the electric field by switching from a stable conductance state to a

current-conducting state in which the second body is in an avalanche breakdown condition and current passes through the second body (FIG. 1-9, 18; [0061-0148, 0231-0243])

Akimoto does not teach a control circuit configured to apply said control signal to the first gate, when the first body is reversed biased, to cause the first body to respond to the electric field by switching from a stable conductance state to a current-conducting state in which the first body is in an avalanche breakdown condition and current passes between the data storage node and the first body. Baba teaches applying a control signal to the first gate, when the first body is reversed biased is known in the art (Col. 2 lines 1-35). This control signal would cause the first body to respond to the electric field by switching from a stable conductance state to a current-conducting state in which the first body is in an avalanche breakdown condition and current passes between the data storage node and the first body in device that has a structure identical to that of which is claimed as is taught by Akimoto. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied a control signal to the device of Akimoto when the body is reversed biased, to cause the first body to respond to the electric field by switching from a stable conductance state to a current-conducting state in which the first body is in an avalanche breakdown condition and current passes between the data storage node and the first body because it is known in the art to control the operation of the transistor by applying a control signal to the gate as taught by Baba (Col. 2 lines 1-35).

Akimoto and Baba do not teach a control circuit configured to apply a control signal. Yee teaches a control circuit configured to apply a control signal to the control/gate electrode to operate a transistor (Col. 2 lines 55-67 and Clm 1). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Akimoto and Baba to have a control circuit to apply the control signal to the gate so that the transistor of Akimoto, which is structurally identical to that which is claimed, can operate as functionally required by the claim using the control circuit as is known in the art and taught by Yee (Col. 2 lines 55-67 and Clm 1).

Claim 31: Akimoto teaches a sense device coupled to the second body and adapted to detect data as a function of sensed current passing through the second body, and wherein the second gate is further adapted to influence an electric field substantially at only one of the first and second junctions ((FIG. 1-9, 18; [0061-0148, 0231-0243])

Claim 32: Akimoto teaches a semiconductor device, comprising: a multi-region body including a first region (142) dominated by charge carriers of a first polarity that extends to a first junction, a second region (143) dominated by charge carriers of a second polarity opposite the first polarity that extends to a second junction, and an intermediate region (144) having an effective length extending from the first junction to the second junction; and first (140) and second (141) gates coupled to the body via intervening dielectric material (FIG. 15; [0071-0072; 00197-0201]).

Akimoto does not teach control circuit configured to apply control signals, when the body is reversed biased (Col. 2 lines 1-35). This control signal when applied to the first and second gates to present an electric field substantially at one of the first and second junctions, to cause the body to respond to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition biased. Baba teaches applying a control signal to a gate, when the body is reversed biased is known in the art (Col. 2 lines 1-35). This control signal and would cause the body to respond to the electric field by switching from a stable conductance state to a current-conducting state in which the first body is in an avalanche breakdown condition and current passes between the data storage node and the first body in device that has a structure identical to that of which is claimed as is taught by Akimoto. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied a control signal to the device of Akimoto when the body is reversed biased, to cause the first body to respond to the electric field by switching from a stable conductance state to a current-conducting state in which the first body is in an avalanche breakdown condition and current passes between the data storage node and the first body because it is known in the art to control the operation of the transistor by applying a control signal to the gate as taught by Baba (Col. 2 lines 1-35).

Akimoto and Baba do not teach a control circuit configured to apply a control signal. Yee teaches a control circuit configured to apply a control signal to the control/gate electrode to operate a transistor (Col. 2 lines 55-67 and Clm 1). Therefore

Art Unit: 2814

it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Akimoto and Baba to have a control circuit to apply the control signal to the gate so that the transistor of Akimoto, which is structurally identical to that which is claimed, can operate as functionally required by the claim using a control circuit as is known in the art and taught by Yee (Col. 2 lines 55-67 and Clm 1).

Claim 33: Akimoto (FIG. 1A-1B; [0071-0072]), Baba and Yee (Col. 2 lines 55-67 and Clm 1) teach the control circuit is configured to apply a control signal to the first gate to capacitively couple a first voltage-bias control signal to the body to accumulate carriers immediately adjacent to said one of the first and second junctions, and to hold the body in a steady state without the avalanche breakdown condition occurring absent a similarly-biased control signal capacitively coupled to the body from the second gate.

Claim 34: Akimoto (FIG. 1A-1B; [0071-0072]), Baba and Yee (Col. 2 lines 55-67 and Clm 1) teach the control circuit is configured to apply a control signal to the first gate to capacitively couple a first voltage-bias control signal to the body to accumulate carriers immediately adjacent to said one of the first and second junctions, and to switch the body the current-conducting state by applying a second voltage-bias control signal capacitively coupled to the body, the first and second voltage-bias control signals being of similar bias.

Claim 35: Akimoto (FIG. 1A-1B; [0071-0072]), Baba and Yee (Col. 2 lines 55-67 and Clm 1) teach the control circuit is responsive to temperature and configured to apply a control signal to the body via the second gate to counter temperature-related

effects that alter the creation of the avalanche breakdown condition in response to a control signal being applied by the first gate.

Claim 36: Akimoto (FIG. 1A-1B; [0071-0072]), Baba and Yee (Col. 2 lines 55-67 and Clm 1) teach the control circuit is configured to apply the control signal to the second gate to maintain a threshold voltage level in the intermediate region, the threshold voltage being a minimum amount of additional voltage applied to the intermediate region for causing the avalanche breakdown condition.

Claim 37: Akimoto teaches an inverter circuit comprising: first (44) and second (43) multi-region bodies, each body having a highly-doped P-type region (23p) that extends to a first junction, a highly-doped N-type region (22p) that extends to a second junction, and an intermediate region (24p) having a neutral polarity relative to the P-type and N-type regions and having a length extending from the first junction to the second junction, the N-type region of the first body and the P-type region of the second body being coupled to a common output node; first (20p) and second (20p) gates respectively capacitively coupled to the first and second bodies (FIG. 1-9, 18; [0061-0148, 0231-0243]).

Akimoto does not teach a control circuit configured to apply control signals to the first and second gates when the bodies are reversed biased, to modulate the length of the intermediate regions of the respective bodies by changing a concentration of carriers in the respective intermediate regions at one of the junctions and offset from the other junction; and an input node coupled to the first and second gates, wherein a change in input signal applied to the input nodes causes an inverted response in an

Art Unit: 2814

output signal at the output node. Baba teaches applying control signals to the gates when the bodies are reversed biased (Col. 2 lines 1-35). This control signal would modulate the length of the intermediate regions of the respective bodies by changing a concentration of carriers in the respective intermediate regions at one of the junctions and offset from the other junction; and an input node coupled to the gates, wherein a change in input signal applied to the input nodes causes an inverted response in an output signal at the output node in a device that has a structure identical to that of which is claimed as is taught by Akimoto. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied control signals to the first and second gates when the bodies are reversed biased, to modulate the length of the intermediate regions of the respective bodies by changing a concentration of carriers in the respective intermediate regions at one of the junctions and offset from the other junction; and an input node coupled to the first and second gates, wherein a change in input signal applied to the input nodes causes an inverted response in an output signal at the output node because it is known in the art to control the operation of a transistor by applying a control signal to the gate as taught by Baba (Col. 2 lines 1-35).

Akimoto and Baba do not teach a control circuit configured to apply a control signal. Yee teaches a control circuit configured to apply a control signal to the control/gate electrode to operate a transistor (Col. 2 lines 55-67 and Clm 1). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Akimoto and Baba to have a control

Art Unit: 2814

circuit to apply the control signal to the gate so that the transistor of Akimoto, which is structurally identical to that which is claimed, can operate as functionally required by the claim using a control circuit as is known in the art and taught by Yee (Col. 2 lines 55-67 and Clm 1).

Claim 39: Akimoto teaches a semiconductor device, comprising: a multi-region body including a first region (22) dominated by charge carriers of a first polarity that extends to a first junction, a second region (23) dominated by charge carriers of a second polarity opposite the first polarity that extends to a second junction, and an intermediate region (24) having an effective length extending from the first junction to the second junction; and a gate for presenting, when the body is reversed biased, an electric field at the first junction and offset from the second junction, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes in the body (FIG. 1A-1B; [0071-0072]).

Akimoto does not teach a gate and a control circuit for presenting, when the body is reversed biased, an electric field at the first junction and offset from the second junction, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes in the body. Baba teaches a gate for presenting, when the body is reversed biased (Col. 2 lines 1-35). This control signal would cause an electric field at the first junction and offset from the second junction, the body responding to the electric field by switching from a stable conductance state to a

Art Unit: 2814

current-conducting state in which the body is in an avalanche breakdown condition and current passes in the body in a device that has a structure identical to that of which is claimed, as is taught by Akimoto. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a gate for presenting, when the body is reversed biased, an electric field at the first junction and offset from the second junction, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes in the body because it is known in the art to control the operation of a transistor by applying a control signal to the gate as taught by Baba (Col. 2 lines 1-35).

Akimoto and Baba do not teach a control circuit presenting. Yee teaches a control circuit configured to apply a control signal to the control/gate electrode to operate a transistor (Col. 2 lines 55-67 and Clm 1). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Akimoto and Baba to have a control circuit to apply the control signal to the gate so that the transistor of Akimoto, which is structurally identical to that which is claimed, can operate as functionally required by the claim using a control circuit as is known in the art and taught by Yee (Col. 2 lines 55-67 and Clm 1).

Claim 43: Akimoto teaches a semiconductor device, comprising: a multi-region body having an upper surface and including a first region (22) dominated by carriers of a first polarity that extends to a first junction, a second region (23) dominated by carriers of an opposite polarity that extends to a second junction, and an intermediate region

(24) having an upper portion over a lower portion and a length extending from the first junction to the second junction; a gate (20) capacitively-coupled to the body (FIG. 1A-1B; [0071-0072]).

Akimoto does not teach a control circuit configured for applying a control signal to the gate, when the body is reversed biased, to cause the gate to modulate the length of the intermediate region by changing a concentration of carriers in a portion of the intermediate region extending from one of the junctions and offset from the other of the junctions and thereby causing the device to transition between a current-conducting state in which the device is in an avalanche breakdown condition and a current-blocking state the avalanche breakdown condition occurring in the lower portion of the intermediate region, the upper portion of the intermediate region being arranged to inhibit hot carriers from the lower portion reaching the upper surface in a current-conducting state. Baba teaches a control circuit configured for applying a control signal to the gate, when the body is reversed biased (Col. 2 lines 1-35). This control signal would then cause the gate to modulate the length of the intermediate region by changing a concentration of carriers in a portion of the intermediate region extending from one of the junctions and offset from the other of the junctions and thereby causing the device to transition between a current-conducting state in which the device is in an avalanche breakdown condition and a current-blocking state the avalanche breakdown condition occurring in the lower portion of the intermediate region, the upper portion of the intermediate region being arranged to inhibit hot carriers from the lower portion reaching the upper surface in a current-conducting state in a device that has a structure

Art Unit: 2814

identical to that of which is claimed, as is taught by Akimoto. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied control signals to the first and second gates when the bodies are reversed biased, to modulate the length of the intermediate regions of the respective bodies by changing a concentration of carriers in the respective intermediate regions at one of the junctions and offset from the other junction; and an input node coupled to the first and second gates, wherein a change in input signal applied to the input nodes causes an inverted response in an output signal at the output node because it is known in the art to control the operation of a transistor by applying a control signal to the gate as is taught by Baba (Col. 2 lines 1-35).

Akimoto and Baba do not teach a control circuit configured to apply a control signal. Yee teaches a control circuit configured to apply a control signal to the control/gate electrode to operate a transistor (Col. 2 lines 55-67 and Clm 1). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Akimoto and Baba to have a control circuit to apply the control signal to the gate so that the transistor of Akimoto, which is structurally identical to that which is claimed, can operate as functionally required by the claim using a control circuit as is known in the art and taught by Yee (Col. 2 lines 55-67 and Clm 1).

Claim 44: Akimoto (FIG. 1A-1B; [0071-0072]) and Yee (Col. 2 lines 55-67 and Clm 1) the control circuit is configured with the body and gates, to apply the control signals to operate the body under subthreshold conditions leading up to switching of the

device between the stable and current-conducting states, in which the subthreshold slope pertaining to a change in current per a corresponding change in voltage is significantly lower than about 60mV/decade.

Claim 45: Akimoto teaches an impact ionization-based semiconductor device, comprising: a multi-region body including a first region, dominated by charge carriers of a first polarity, that extends to a first junction, a second region, dominated by charge carriers of a second polarity opposite the first polarity, that extends to a second junction, and an intermediate region having an effective length extending from the first junction to the second junction; first and second gates coupled to the body via intervening dielectric material (FIG. 15; [0071-0072; 00197-0201]).

Akimoto does not teach a control circuit configured to apply control signal, when the body is reversed biased, to the respective first and second gates to generate an electric field substantially at one of the first and second junctions, and to cause the body to switch from a stable conductive state to a current-conducting state in which the body is in an avalanche breakdown condition. Baba teaches applying a control signal when the body is reversed biased (Col. 2 lines 1-35). This control signal would cause first and second gates to generate an electric field substantially at one of the first and second junctions, and to cause the body to switch from a stable conductive state to a current-conducting state in which the body is in an avalanche breakdown condition in a device that has a structure identical to that of which is claimed, as is taught by Akimoto. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a gate for presenting, when the body is reversed biased, to

Art Unit: 2814

the respective first and second gates to generate an electric field substantially at one of the first and second junctions, and to cause the body to switch from a stable conductive state to a current-conducting state in which the body is in an avalanche breakdown condition because it is known in the art to control the operation of a transistor by applying a control signal to the gate as taught by Baba (Col. 2 lines 1-35).

Akimoto and Baba do not teach a control circuit presenting. Yee teaches a control circuit configured to apply a control signal to the control/gate electrode to operate a transistor (Col. 2 lines 55-67 and Clm 1). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Akimoto and Baba to have a control circuit to apply the control signal to the gate so that the transistor of Akimoto, which is structurally identical to that which is claimed, can operate as functionally required by the claim using a control circuit as is known in the art and taught by Yee (Col. 2 lines 55-67 and Clm 1).

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto (US PGPub 2002/0117689), Baba et al. (US Patent 5,686,739) and Yee et al. (US Patent 5,736,890), as applied to claim 1 above, and further in view of Baba (US Patent 5,589,696 of record).

Regarding claim 8, as described above, Akimoto, Baba ('739) and Yee substantially read on the invention as claimed, except Akimoto and Yee do not teach the gate is located at least predominantly over the second region. Baba ('696) teaches the gate (21) is located at least predominantly over the second region (FIG. 2) to be

Art Unit: 2814

more highly integrated (Col. 4 lines 1-20). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Akimoto, Baba ('739) and Yee to have the gate located predominantly over the second region to be more highly integrated as taught by Baba ('696) (Col. 4 lines 1-20).

5. Claims 21-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizutani (US Patent 5,616,944 of record) in view of Baba (US Patent 5,589,696 of record) and Yee et al. (US Patent 5,736,890)

Claim 21: Mizutani teaches a memory circuit comprising: a data storage node; a multi-region body including a first region dominated by charge carriers of a first polarity that extends to a first junction, a second region dominated by charge carriers having a second and opposite polarity that extends to a second junction, and an intermediate region having an effective length extending from the first junction to the second junction, the gate being coupled to the body via an intervening dielectric material (FIG. 1; Col. 3-5).

Mizutani does not teach the gate being offset, and a control signal applied via the gate. Baba ('696) teaches a gate (21) offset and used to apply a control signal to the device when the body is reversed bias. This control signal would to present an electric field substantially at only one of the two junctions (13/11 and 15/11) (FIG. 1, 2) creating offset current in the reverse biased mode (Col. 3 lines 1-15, Col. 4 lines 1-15). Further the control signal would present an electric field substantially at only one of the first and

Art Unit: 2814

second junctions, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node in the body of a device that has a structure identical to that of which is claimed, as is taught by Mizutani. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Mizutani to have the gate located predominantly over the second region to create and offset current at only one of the two junctions in the reverse biased mode as taught by Baba ('696) (Col. 3 lines 1-15).

Mizutani and Baba do not teach a control circuit for applying a control signal to the gate electrode. Yee teaches a control circuit configured to apply a control signal to the control/gate electrode to operate a transistor (Col. 2 lines 55-67 and Clm 1).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Mizutani and Baba to have a control circuit to apply the control signal to the gate so that the transistor of Mizutani, which is structurally identical to that which is claimed, can operate as functionally required by the claim using a control circuit as is known in the art and taught by Yee (Col. 2 lines 55-67 and Clm 1).

Claim 22: Mizutani (FIG. 1; Col. 3-5) and Yee (Col. 2 lines 55-67 and Clm 1) teach the body and the control circuit are adapted to access data stored at the data storage node as a function of the avalanche breakdown condition.

Claim 23: Mizutani (FIG. 1; Col. 3-5) and Yee (Col. 2 lines 55-67 and Clm 1) teach the body and the control circuit are adapted to read data from the data storage node as a function of the avalanche breakdown condition.

Claim 24: Mizutani (FIG. 1; Col. 3-5) and Yee (Col. 2 lines 55-67 and Clm 1) teach the body and the control circuit are configured to write data to the data storage node as a function of the avalanche breakdown condition.

Claim 25: Mizutani (FIG. 1; Col. 3-5) and Yee (Col. 2 lines 55-67 and Clm 1) the control circuit maintains a charge at the data storage node by applying the control signal to control the body in a reverse biased condition.

Claim 26: Mizutani teaches the body and the storage nodes are adapted to drain a charge at the storage node in response to the body being placed in a forward biased condition (FIG. 1; Col. 3-5).

Claim 27: Mizutani teaches a memory circuit comprising: a data storage node; a multi-region body including a first region dominated by charge carriers having a first polarization that extends to a first junction, a second region dominated by charge carriers having a second polarity that is opposite the first polarity that extends to a second junction, and an intermediate region having an effective length extending from the first junction to the second junction (FIG. 1; Col. 3-5).

Mizutani does not teach the gate being offset, and a control signal applied via the gate. Baba ('696) teaches a gate (21) offset and used to apply a control signal to the device when the body is reversed bias. This control signal would to present an electric field substantially at only one of the two junctions (13/11 and 15/11) (FIG. 1, 2) creating

Art Unit: 2814

offset current in the reverse biased mode (Col. 3 lines 1-15, Col. 4 lines 1-15). Further the control signal would present an electric field substantially at only one of the first and second junctions, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node in the body of a device that has a structure identical to that of which is claimed, as is taught by Mizutani. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Mizutani to have the gate located predominantly over the second region to create and offset current at only one of the two junctions in the reverse biased mode as taught by Baba ('696) (Col. 3 lines 1-15).

Mizutani and Baba do not teach a control circuit for applying a control signal to the gate electrode. Yee teaches a control circuit configured to apply a control signal to the control/gate electrode to operate a transistor (Col. 2 lines 55-67 and Clm 1).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Mizutani and Baba to have a control circuit to apply the control signal to the gate so that the transistor of Mizutani, which is structurally identical to that which is claimed, can operate as functionally required by the claim using a control circuit as is known in the art and taught by Yee (Col. 2 lines 55-67 and Clm 1).

Claim 28: Mizutani teaches the data storage node is coupled to the gate, the gate responding to a charge at the data storage node by presenting the electric field (FIG. 1; Col. 3-5).

Claim 29: Mizutani teaches a sense device coupled to the body and adapted to detect data stored at the data storage node in response to current passing through the body (FIG. 1; Col. 3-5).

Claim 38: Mizutani teaches a semiconductor device comprising: a relatively thin intermediate region defined by sides including an upper portion and a sidewall portion; a first region dominated by a first polarization that extends to a first junction with the intermediate region; a second region dominated by a second polarization that extends to a second junction with the intermediate region; and a gate extending around and capacitively coupled to at least two sides of the intermediate region for coupling a voltage to the intermediate region (Fig. 1b, Col. 2-3).

Mizutani does not teach a control circuit configured to apply a control signal to the gate, when the first and second regions are reversed biased, to cause the gate to present an electric field substantially at only one of the first and second junctions, and to cause the device to respond to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes through the intermediate region. Baba ('696) teaches applying a control signal to the device when the body is reversed bias. This control signal would to present an electric field substantially at only one of the two junctions (13/11 and 15/11) (FIG. 1, 2) creating offset current in the reverse biased mode (Col. 3

Art Unit: 2814

lines 1-15, Col. 4 lines 1-15). Further the control signal would present an electric field substantially at only one of the first and second junctions, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node in the body of a device that has a structure identical to that of which is claimed, as is taught by Mizutani. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Mizutani to have the gate located predominantly over the second region to create and offset current at only one of the two junctions in the reverse biased mode as taught by Baba ('696) (Col. 3 lines 1-15).

Mizutani and Baba do not teach a control circuit for applying a control signal to the gate electrode. Yee teaches a control circuit configured to apply a control signal to the control/gate electrode to operate a transistor (Col. 2 lines 55-67 and Clm 1).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Mizutani and Baba to have a control circuit to apply the control signal to the gate so that the transistor of Mizutani, which is structurally identical to that which is claimed, can operate as functionally required by the claim using a control circuit as is known in the art and taught by Yee (Col. 2 lines 55-67 and Clm 1).

Response to Arguments

6. Applicant's arguments with respect to claims 1-7, 9-17, 18-29, 32-39 and 43-45 have been considered but are moot in view of the new ground(s) of rejection.

It is noted that the claim limitations “a control circuit configured to apply a control signal, when the body is reversed biased, to modulate the effective length of the intermediate region to a nonzero value by changing a concentration of carriers in a portion of the intermediate region extending from the second junction and offset from the first junction” or “to switch between two stable conductance states” or “to present an electric field substantially at only one of the first and second junctions, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node and the body”, etc. are considered a method of operating the semiconductor device being claimed. Because the claims submitted are product/device claims, limitations regarding methods of operating the device are not given patentable weight, but are hereby considered and rejected using the reference combination above. It is further noted that where the claimed and prior art products are identical or substantially identical in structure or composition or are produced by identical or substantially identical processes, claimed properties or functions are presumed to be inherent. In re Best, 195 USPQ 430, 433 (CCPA 1977). It has also been held that products of identical chemical composition cannot have mutually exclusive properties. A chemical composition and its properties are inseparable. Therefore, if the prior arts teach the identical chemical structure the

Art Unit: 2814

properties applicant discloses and/or claims are necessarily present. In re Spada, 15 USPQ 2d 1655, 1658 (Fed. Cir. 1990). Akimoto/Mizutani teach the structure of the device as required by the claim limitations, therefore would function as required when a control signal is applied by a control circuit when the device is in reversed bias mode. Baba and Yee show that it is known in the art to use a control signal to apply a control signal to a gate/control electrode so that the device can be operational as is allowed by the device structure.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sarah K Salerno whose telephone number is (571)270-1266. The examiner can normally be reached on M-R 8:00-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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